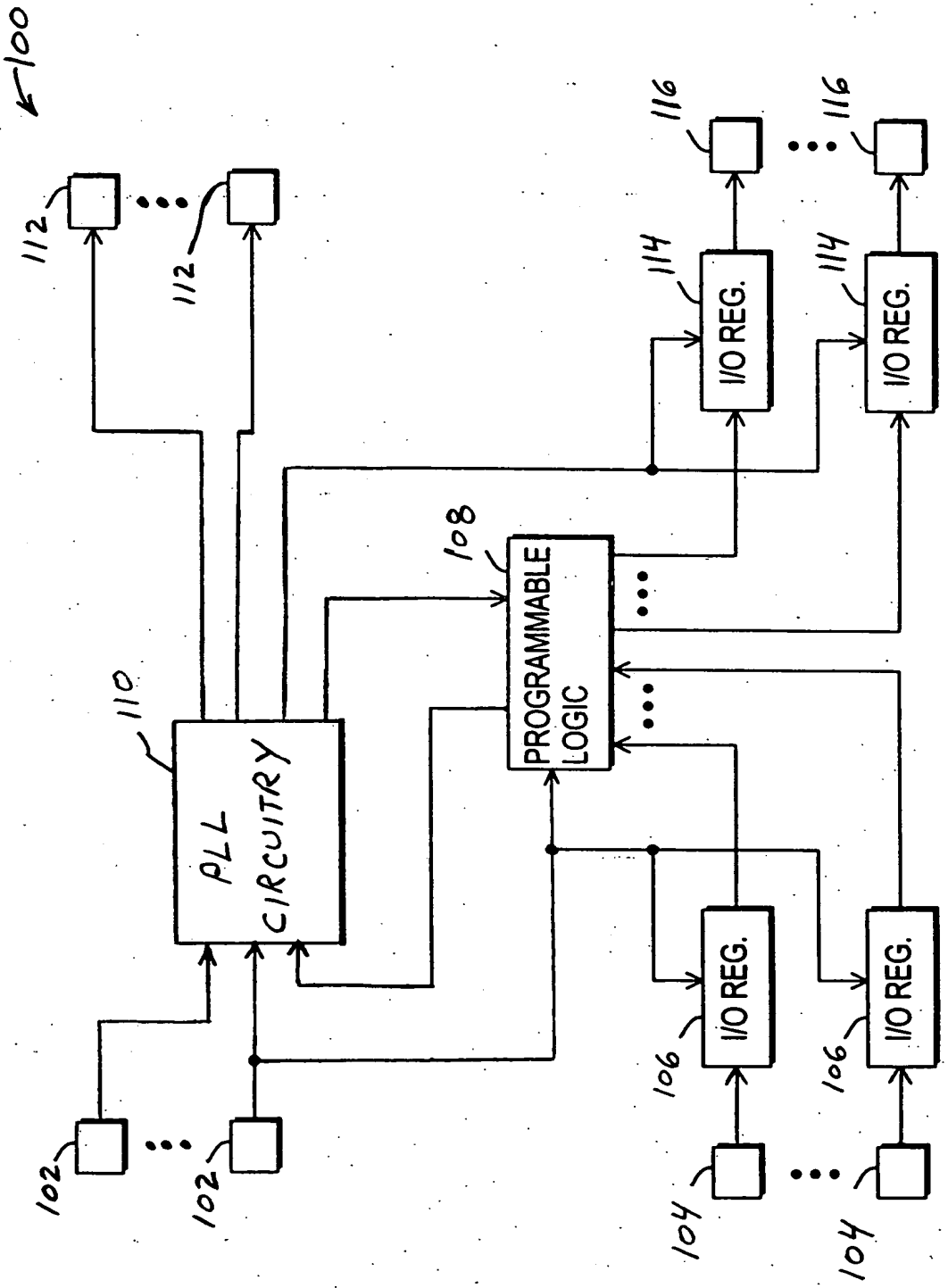
100
112
112
116
116
114
114
I/O REG.
I/O REG.
108
PROGRAMMABLE LOGIC
110
PLL CIRCUITRY
106
106
I/O REG.
I/O REG.
102
102
104
104

FIG. 1

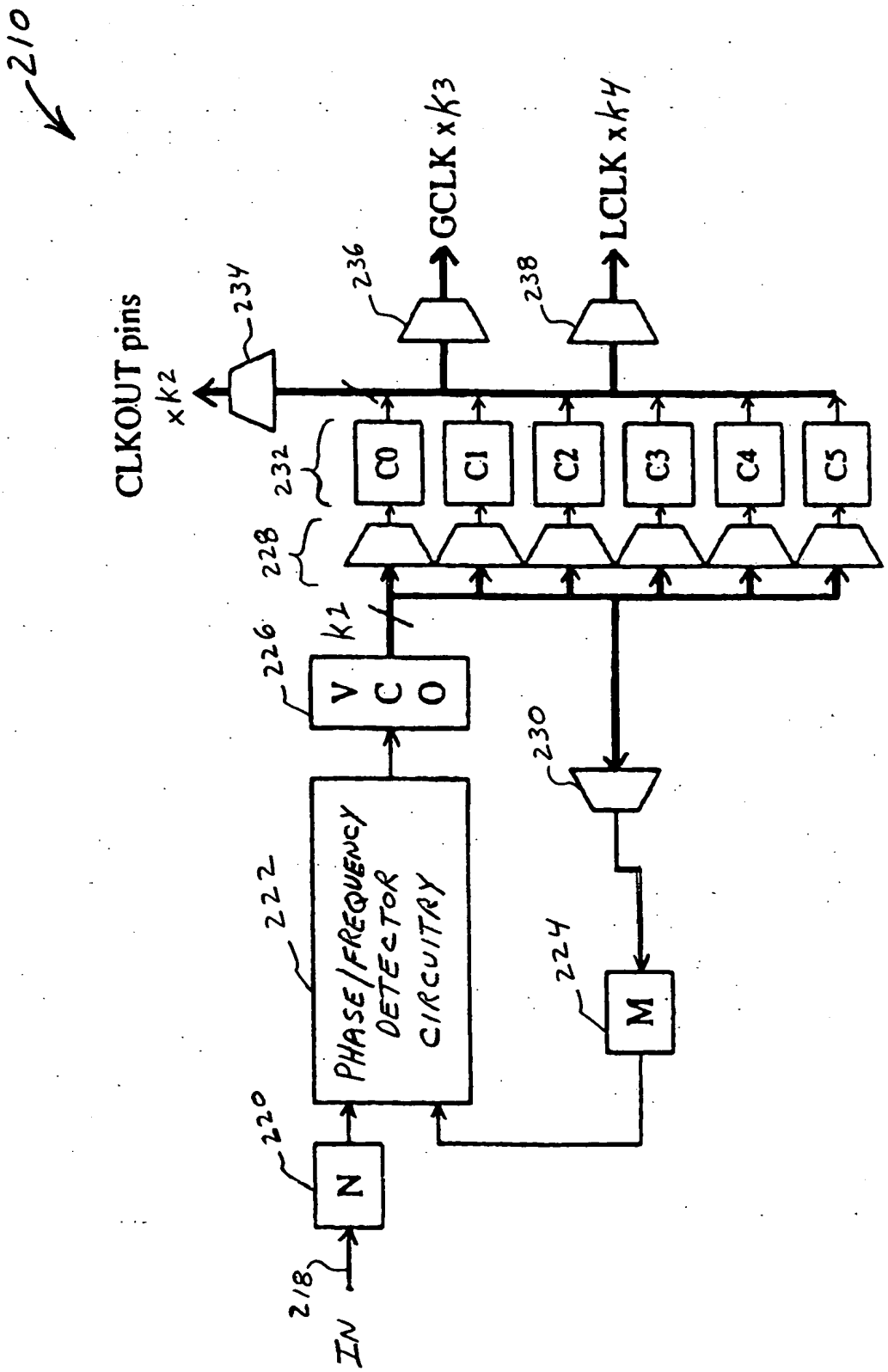
210
CLKOUT pins
xK2
234
GCLK xK3
236
LCLK xK4
238
232
C0
C1
C2
C3
C4
C5
228
226
VCO
K1
230
PHASE/FREQUENCY DETECTOR CIRCUITRY
222
224
M
220
N
218
IN

FIG. 2

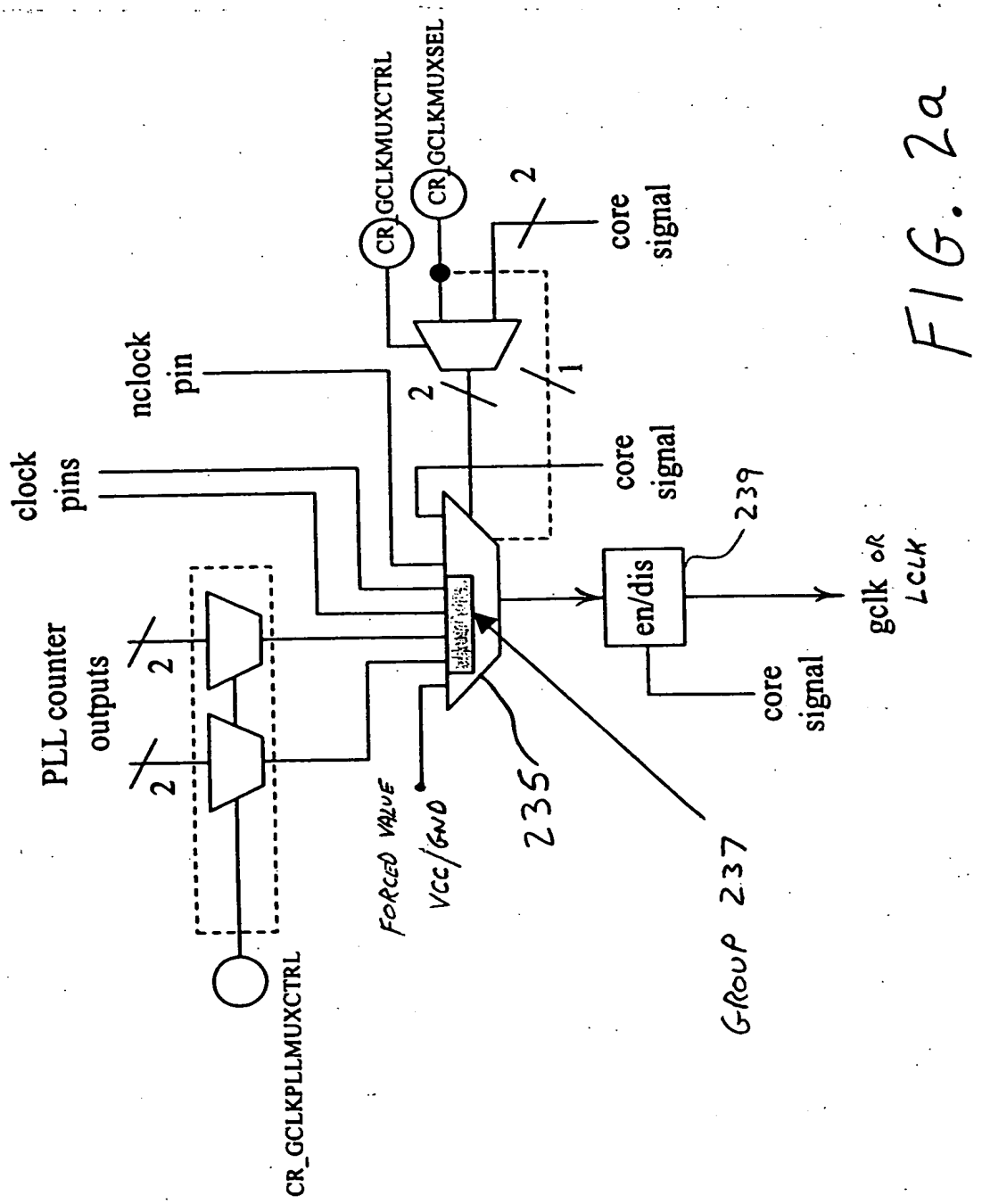
CR GCLKMUXCTRL
CR GCLKMUXSEL
2
core signal
nclock pin
clock pins
2
1
core signal
239
en/dis
gclk or LCLK
core signal
PLL counter outputs
2
2
FORCED VALUE
VCC/GND
235
GROUP 237
CR_GCLKPLLMUXCTRL

FIG. 2a

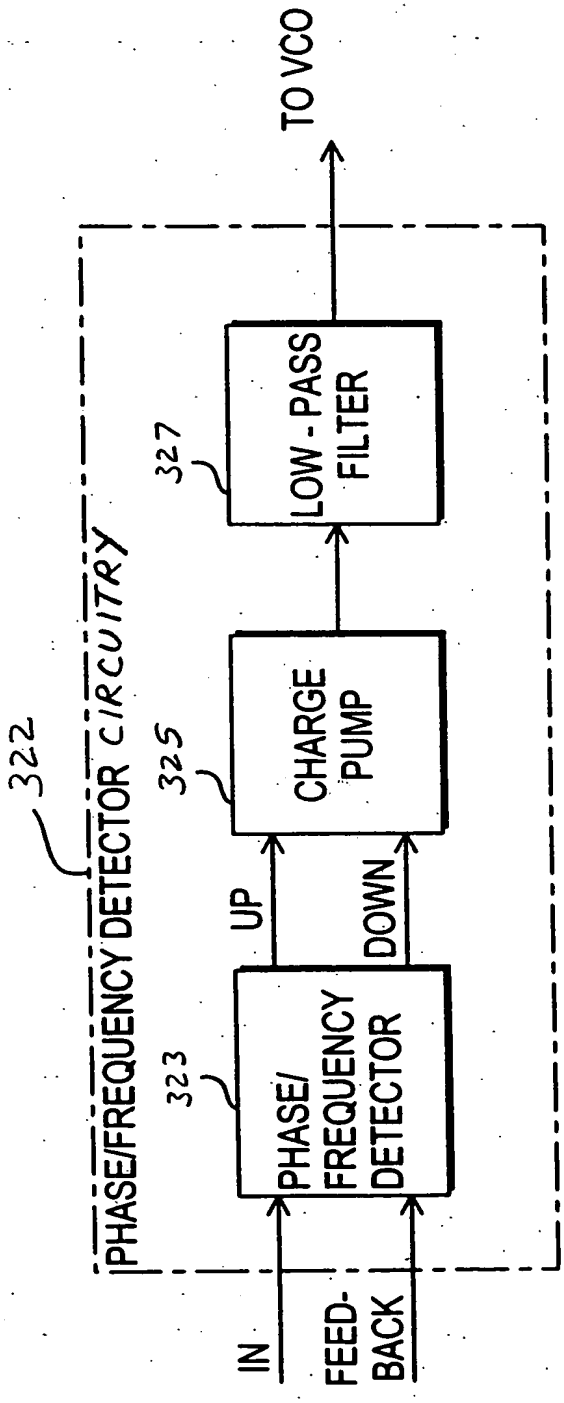
TO VCO
322
PHASE/FREQUENCY DETECTOR CIRCUITRY
327
LOW-PASS FILTER
325
CHARGE PUMP
UP
DOWN
323
PHASE/ FREQUENCY DETECTOR
IN
FEED-BACK

FIG. 3

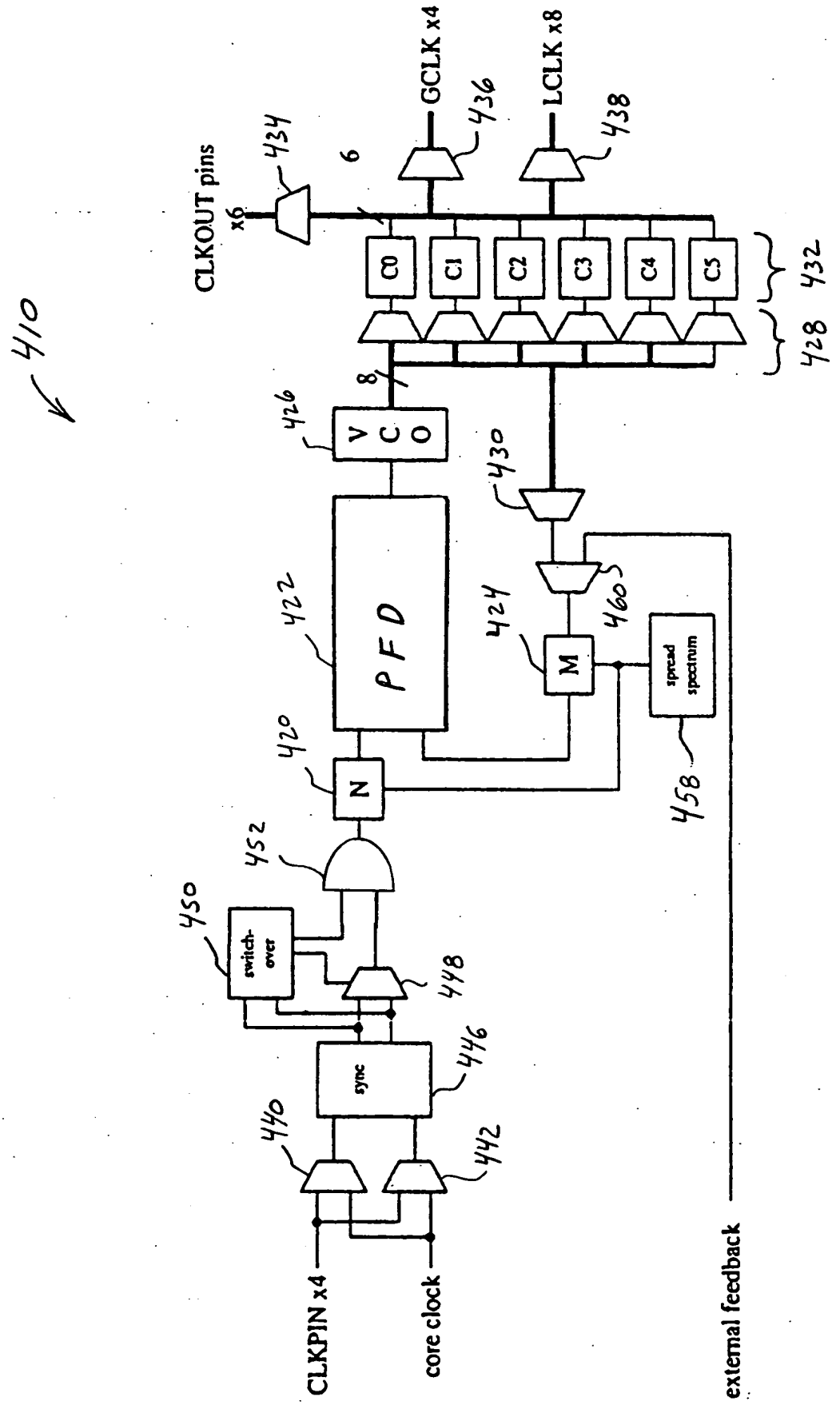
410
CLKOUT pins
x6
434
6
GCLK x4
436
LCLK x8
438
C0
C1
C2
C3
C4
C5
432
428
8
426
VCO
430
422
PFD
424
M
460
spread spectrum
420
N
458
452
450
switch-over
448
446
sync
440
442
CLKPIN x4
core clock
external feedback

FIG. 4

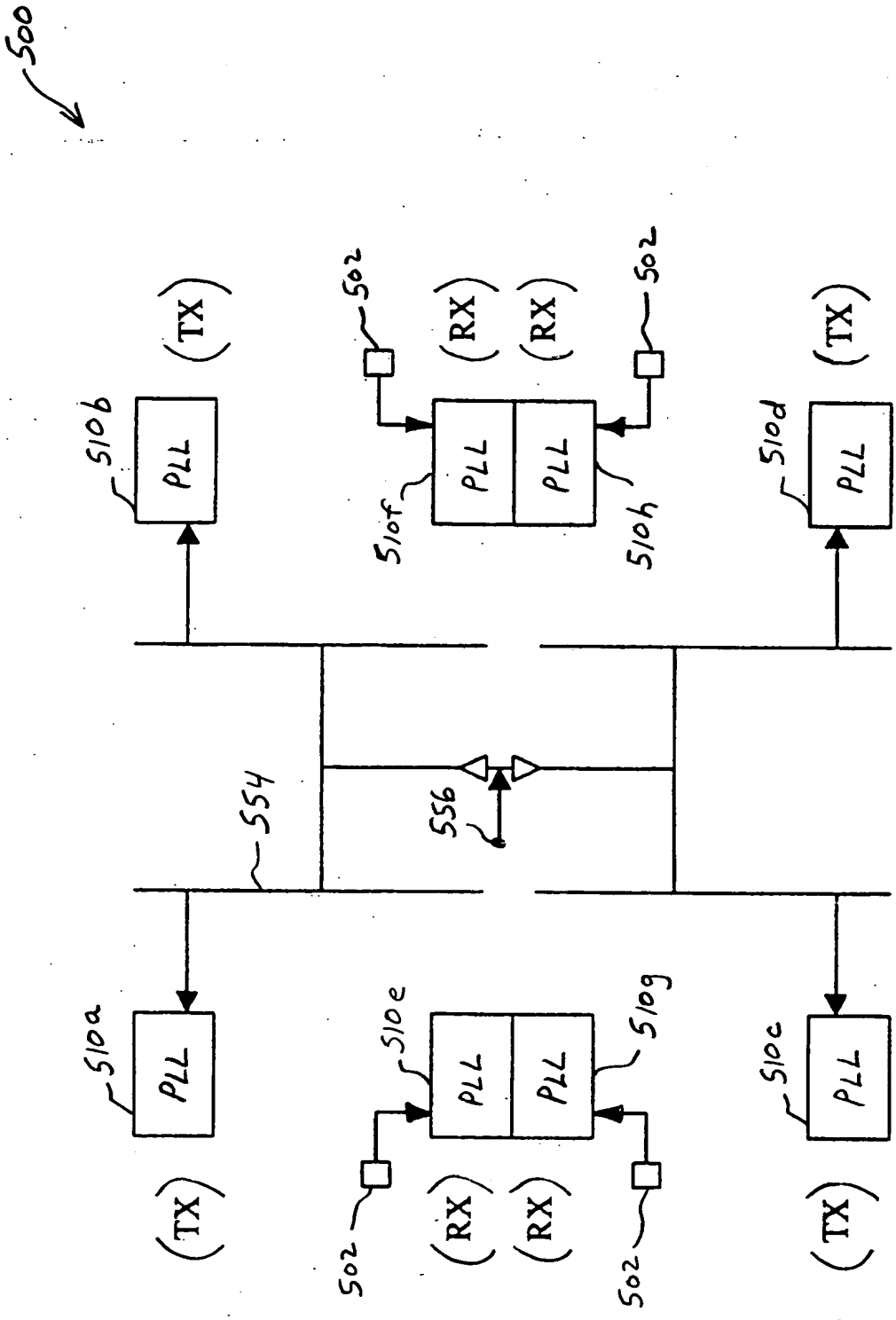
500
502
(TX)
(RX)
(RX)
502
(TX)
510b
PLL
510f
PLL
PLL
510h
510d
PLL
554
556
510a
PLL
510e
PLL
PLL
510g
510c
PLL
502
(TX)
(RX)
(RX)
502
(TX)

FIG. 5

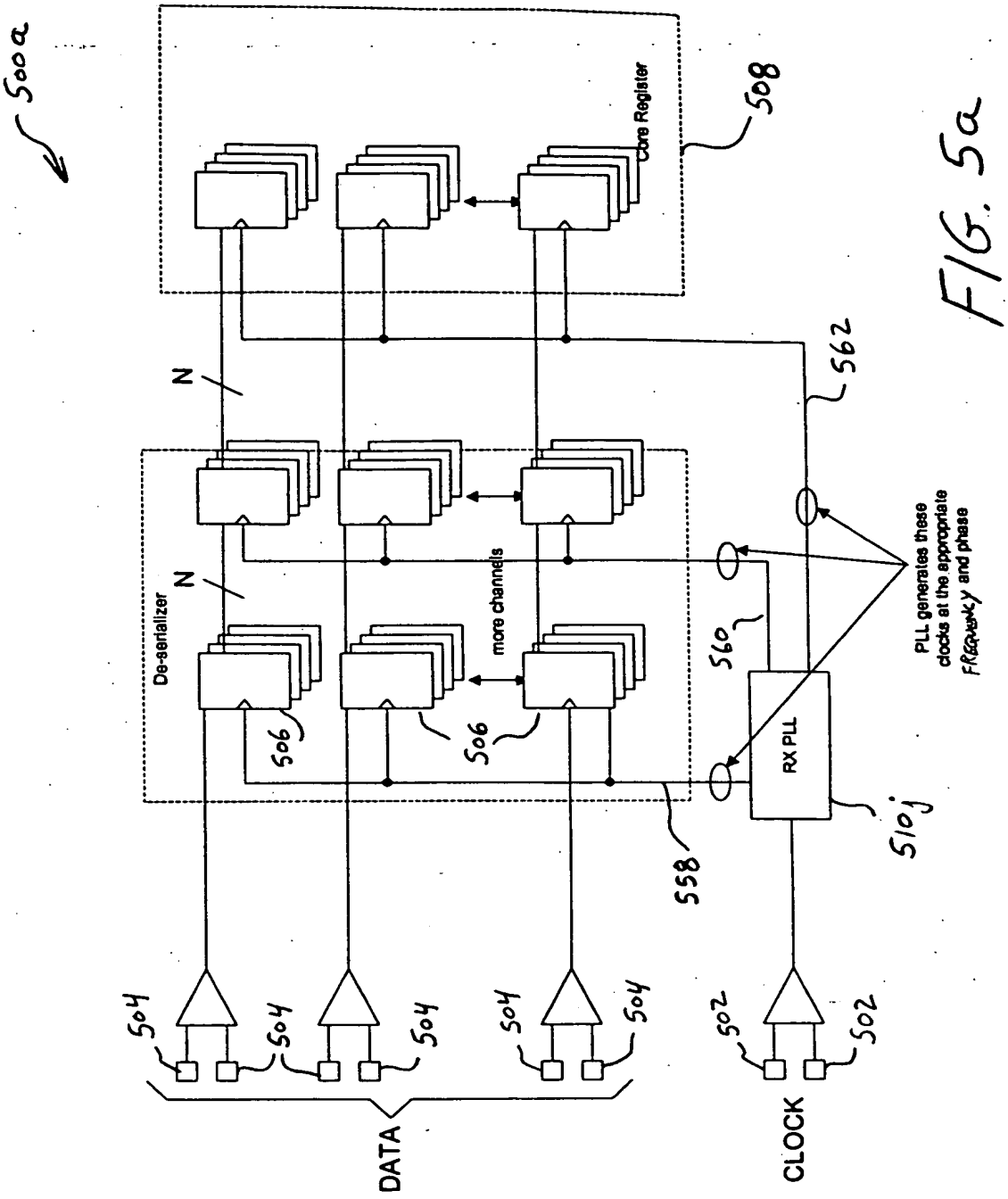
500a
508
Core Register
562
N
N
De-serializer
more channels
560
PLL generates these clocks at the appropriate frequency and phase
506
506
558
RX PLL
510j
504
504
504
504
504
502
502
DATA
CLOCK

FIG. 5a

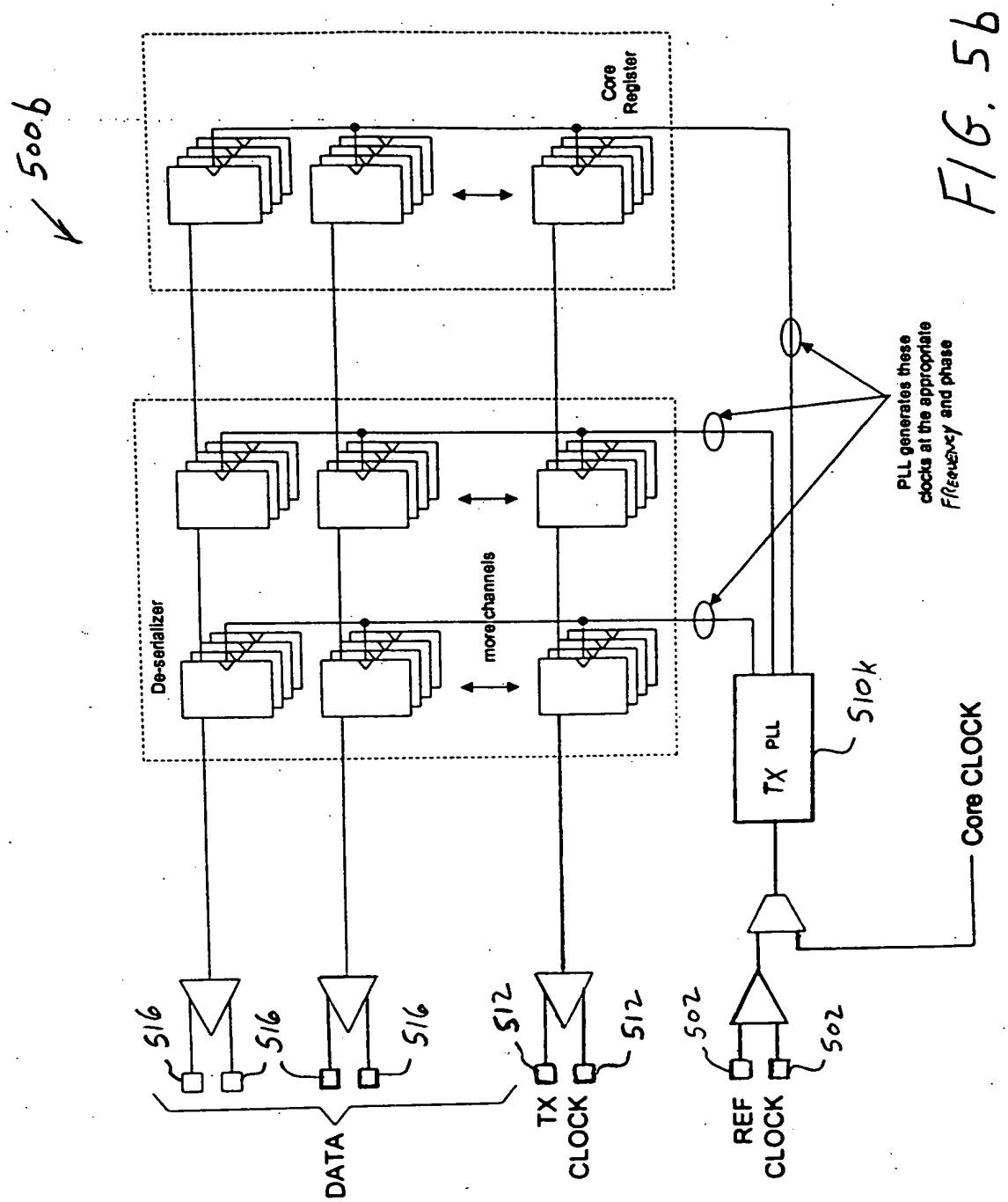
500b
Core Register
De-serializer
more channels
PLL generates these clocks at the appropriate frequency and phase
TX PLL
510k
Core CLOCK
516
516
516
512
512
502
502
DATA
TX CLOCK
REF CLOCK

FIG. 5b

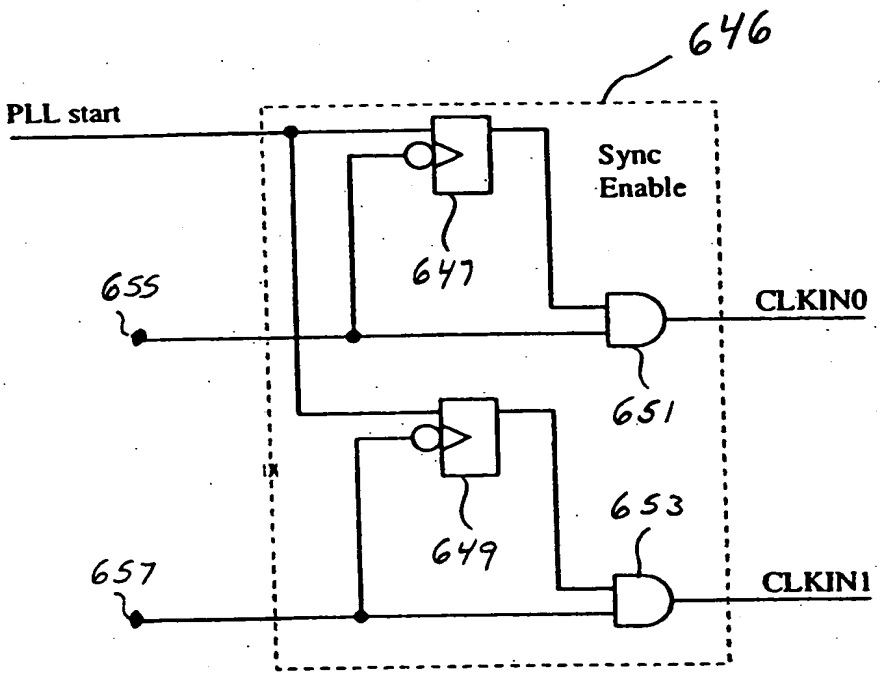
646
PLL start
Sync
Enable
647
655
CLKIN0
651
653
649
657
CLKIN1

FIG. 6

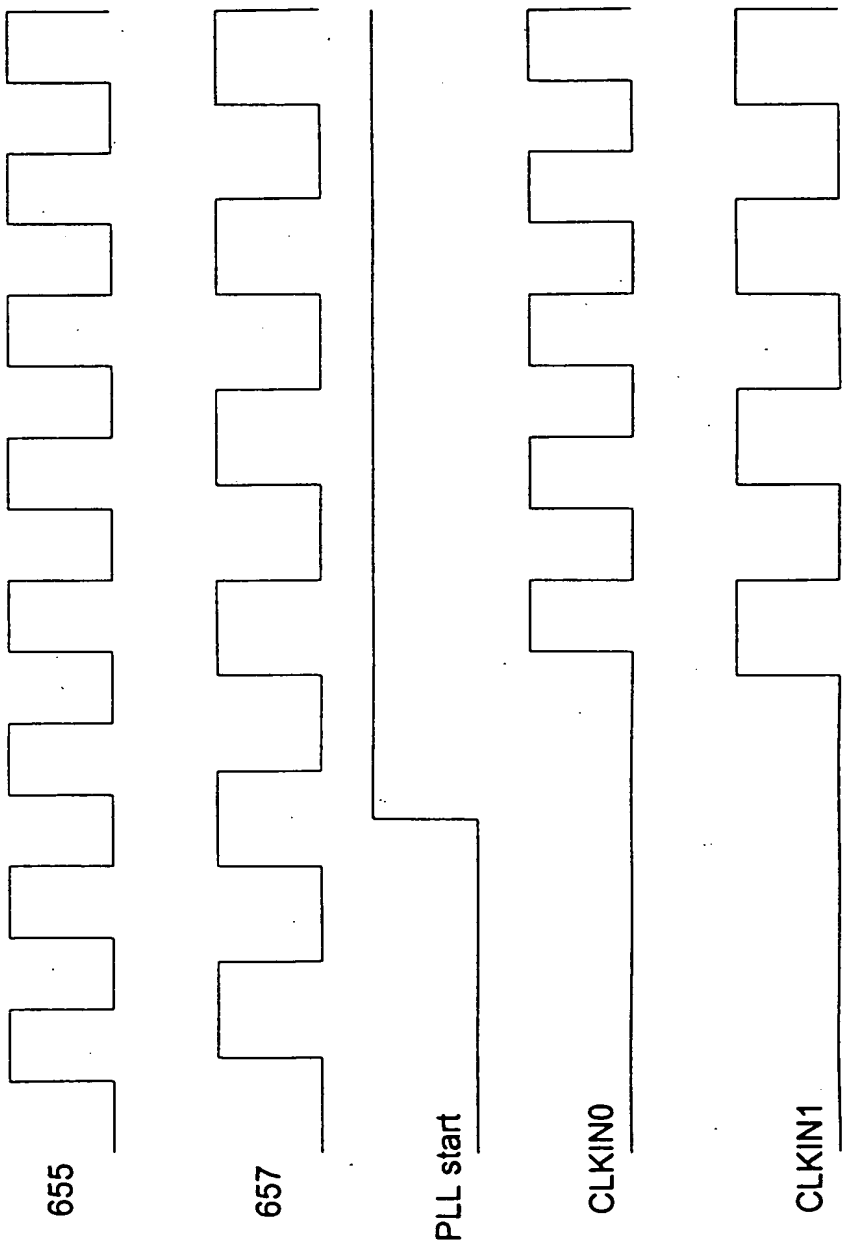

FIG. 6a

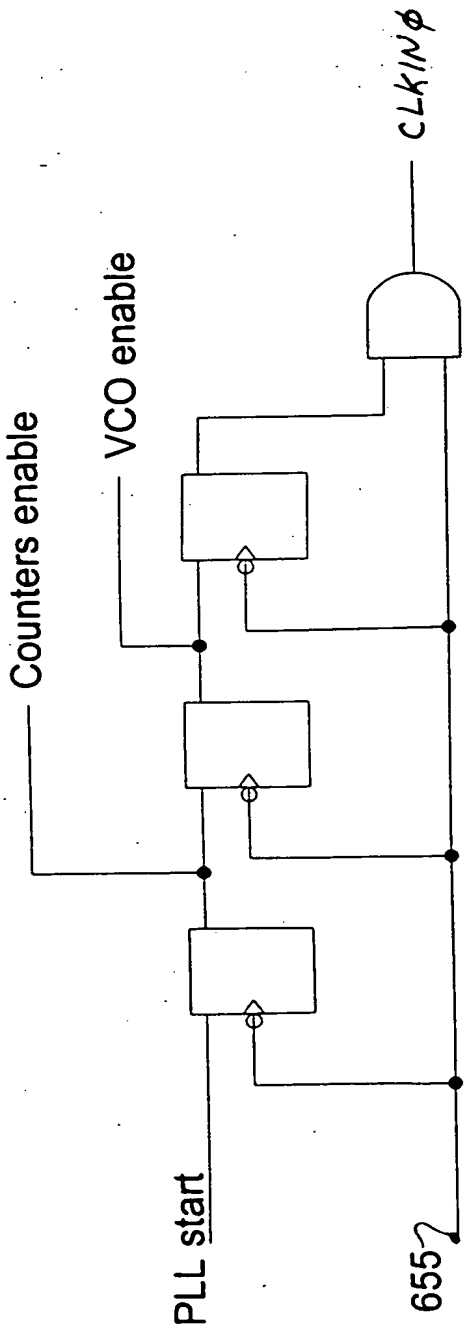

FIG. 6b

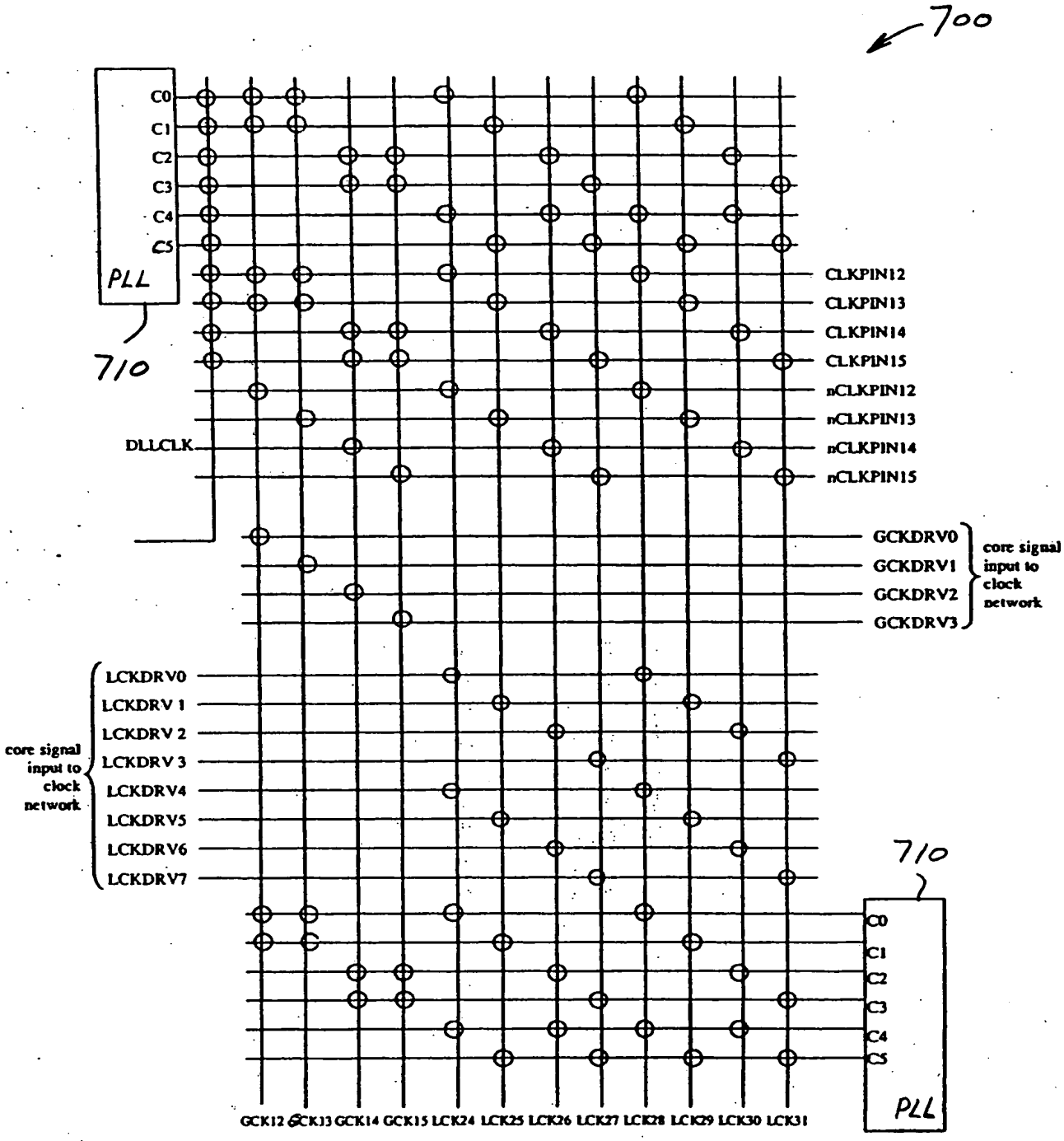
700
C0
C1
C2
C3
C4
C5
PLL
710
DLLCLK
CLKPIN12
CLKPIN13
CLKPIN14
CLKPIN15
nCLKPIN12
nCLKPIN13
nCLKPIN14
nCLKPIN15
GCKDRV0
GCKDRV1
GCKDRV2
GCKDRV3
core signal input to clock network
LCKDRV0
LCKDRV 1
LCKDRV 2
LCKDRV 3
LCKDRV4
LCKDRV5
LCKDRV6
LCKDRV7
core signal input to clock network
710
C0
C1
C2
C3
C4
C5
PLL
GCK12 GCK13 GCK14 GCK15 LCK24 LCK25 LCK26 LCK27 LCK28 LCK29 LCK30 LCK31

FIG. 7

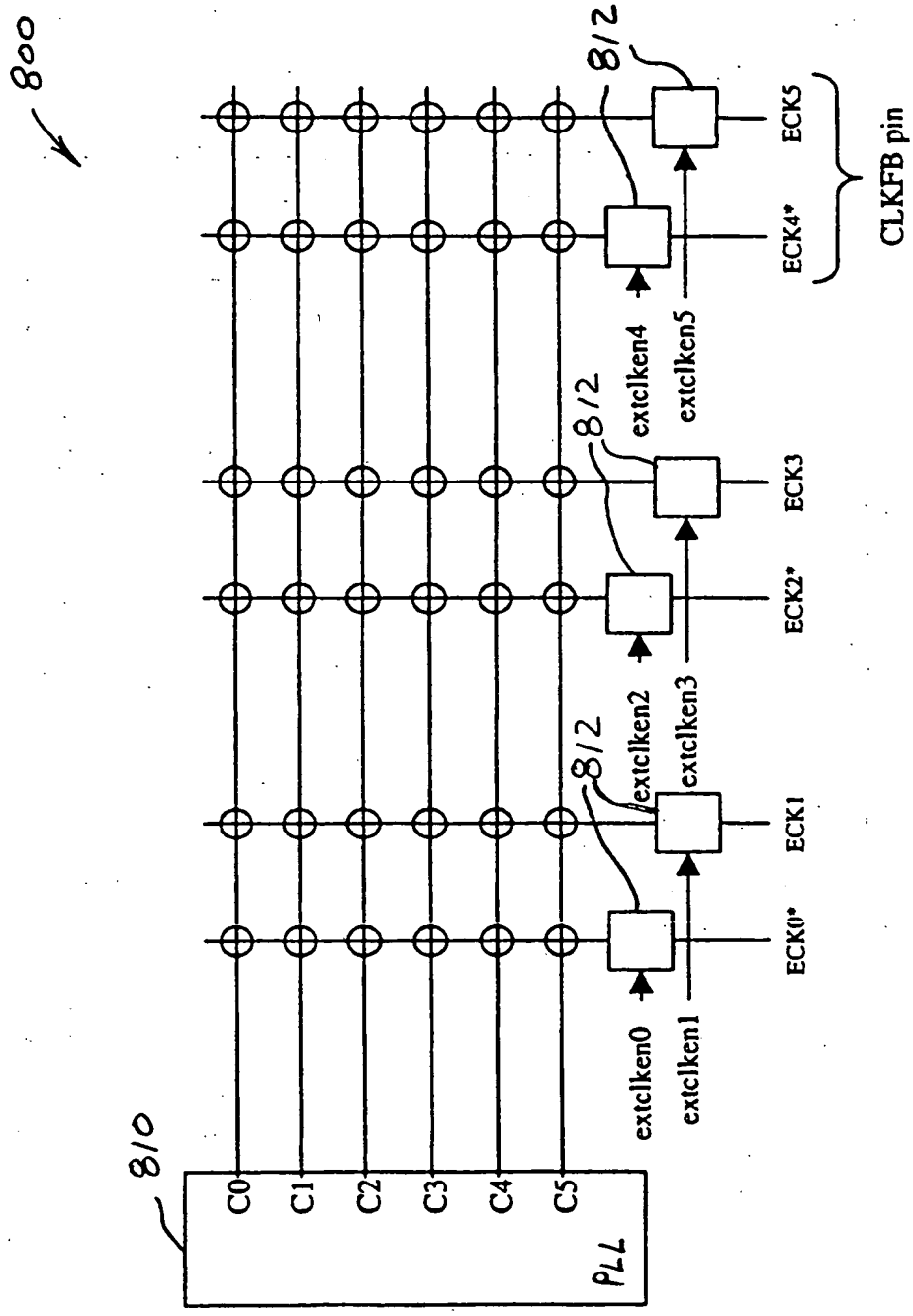
800
812
812
812
ECK5
ECK4*
CLKFB pin
extclken4
extclken5
ECK3
ECK2*
extclken2
extclken3
ECK1
ECK0*
extclken0
extclken1
810
C0
C1
C2
C3
C4
C5
PLL
* denotes the differential output source

FIG. 8

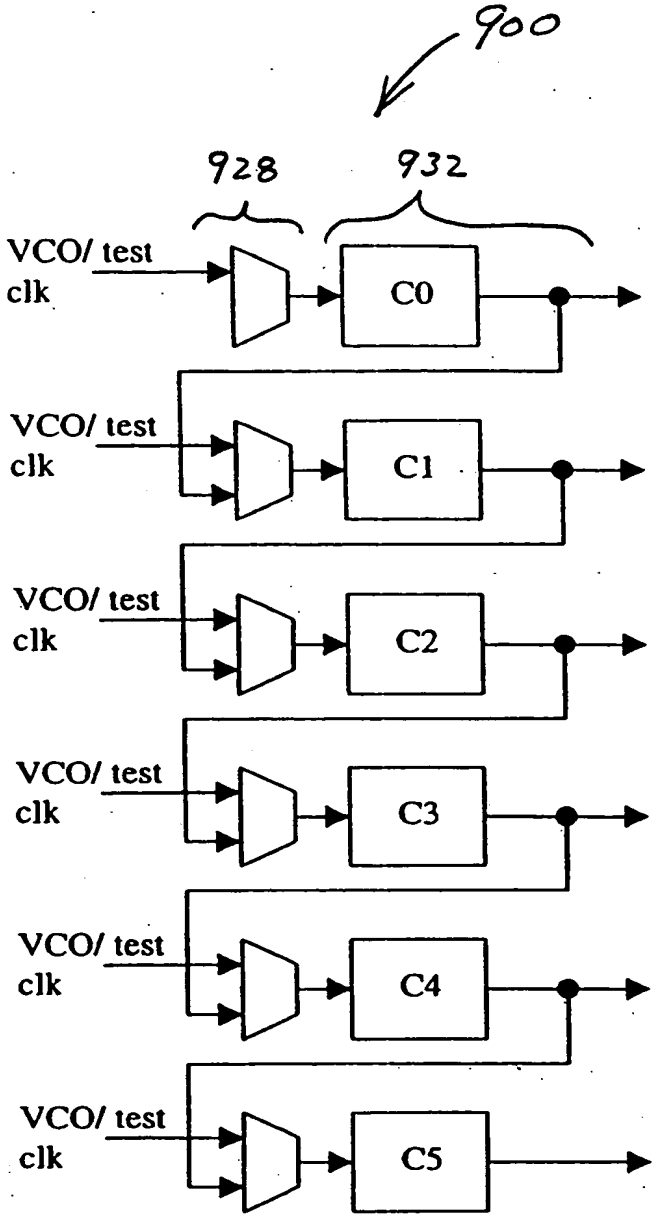
900
928
932
VCO/ test clk
C0
VCO/ test clk
C1
VCO/ test clk
C2
VCO/ test clk
C3
VCO/ test clk
C4
VCO/ test clk
C5

FIG. 9

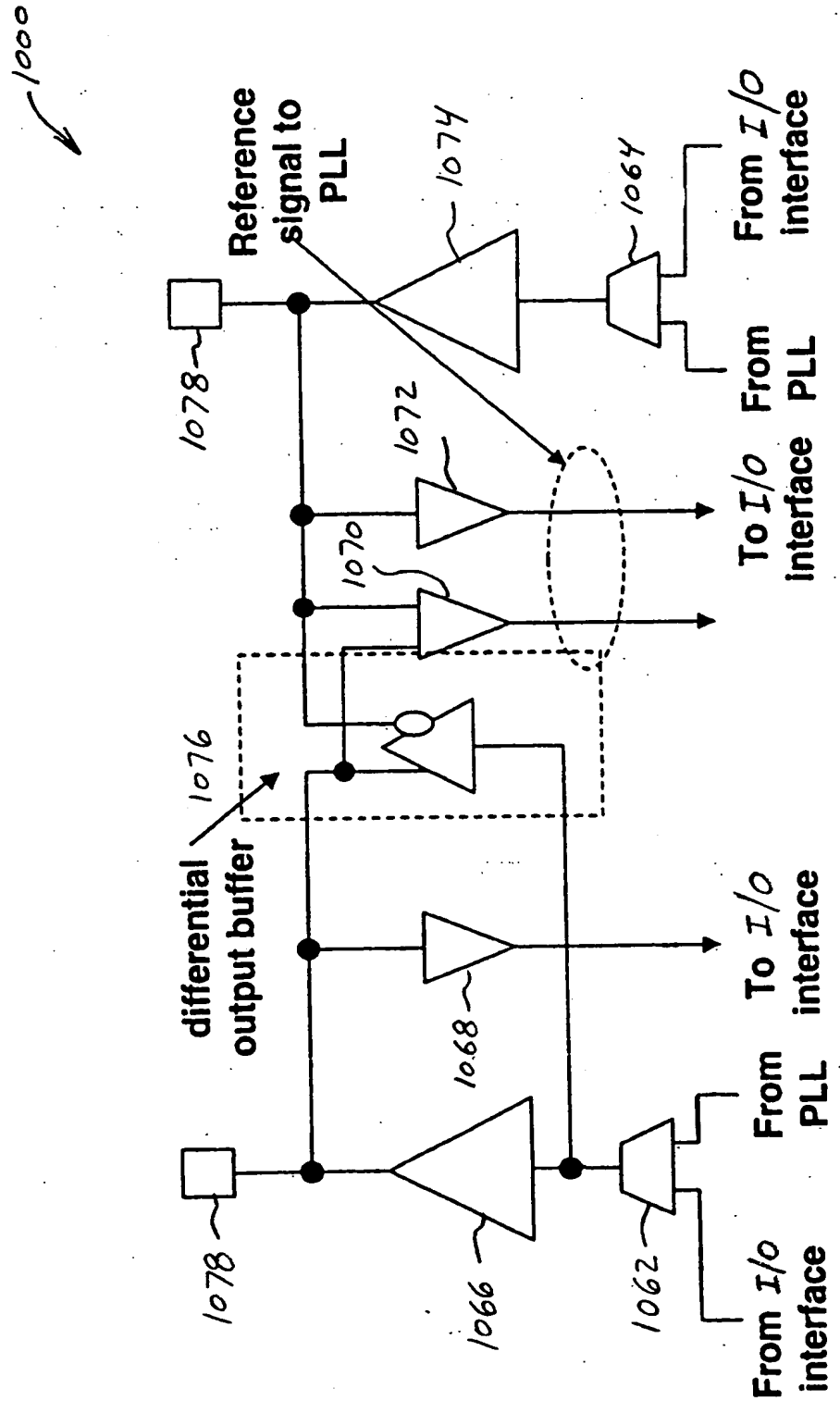
1000
Reference signal to PLL
1074
1064
From I/O interface
From PLL
1078
1072
To I/O interface
1070
1076
differential output buffer
To I/O interface
1068
From PLL
1078
1066
1062
From I/O interface

FIG. 10

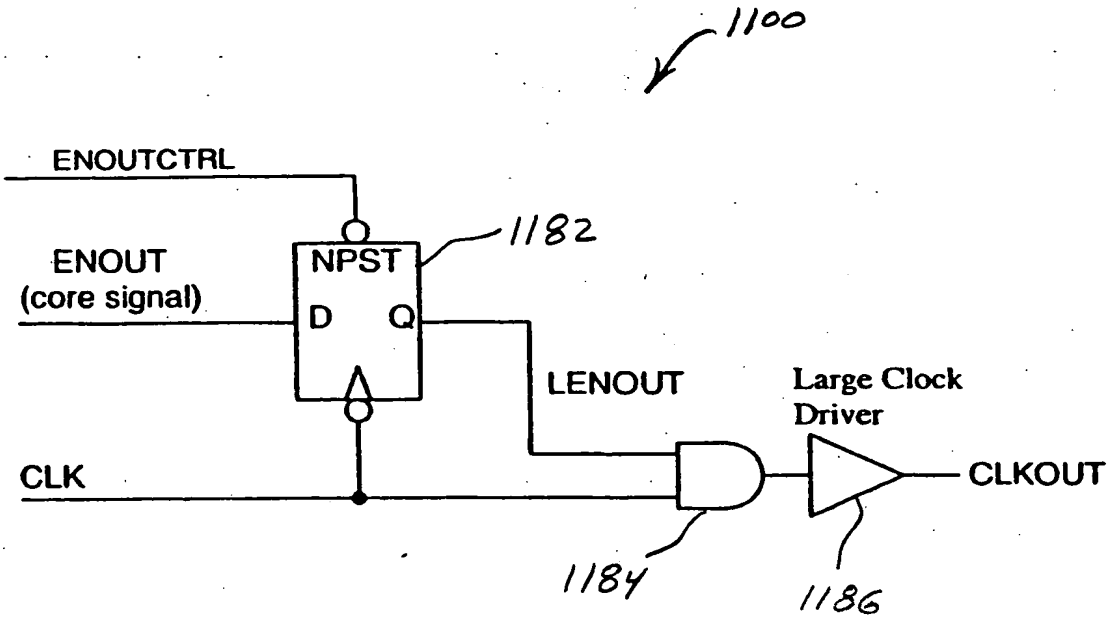
1100
ENOUTCTRL
ENOUT
(core signal)
NPST
D
Q
1182
LENOUT
Large Clock
Driver
CLK
CLKOUT
1184
1186

FIG. 11

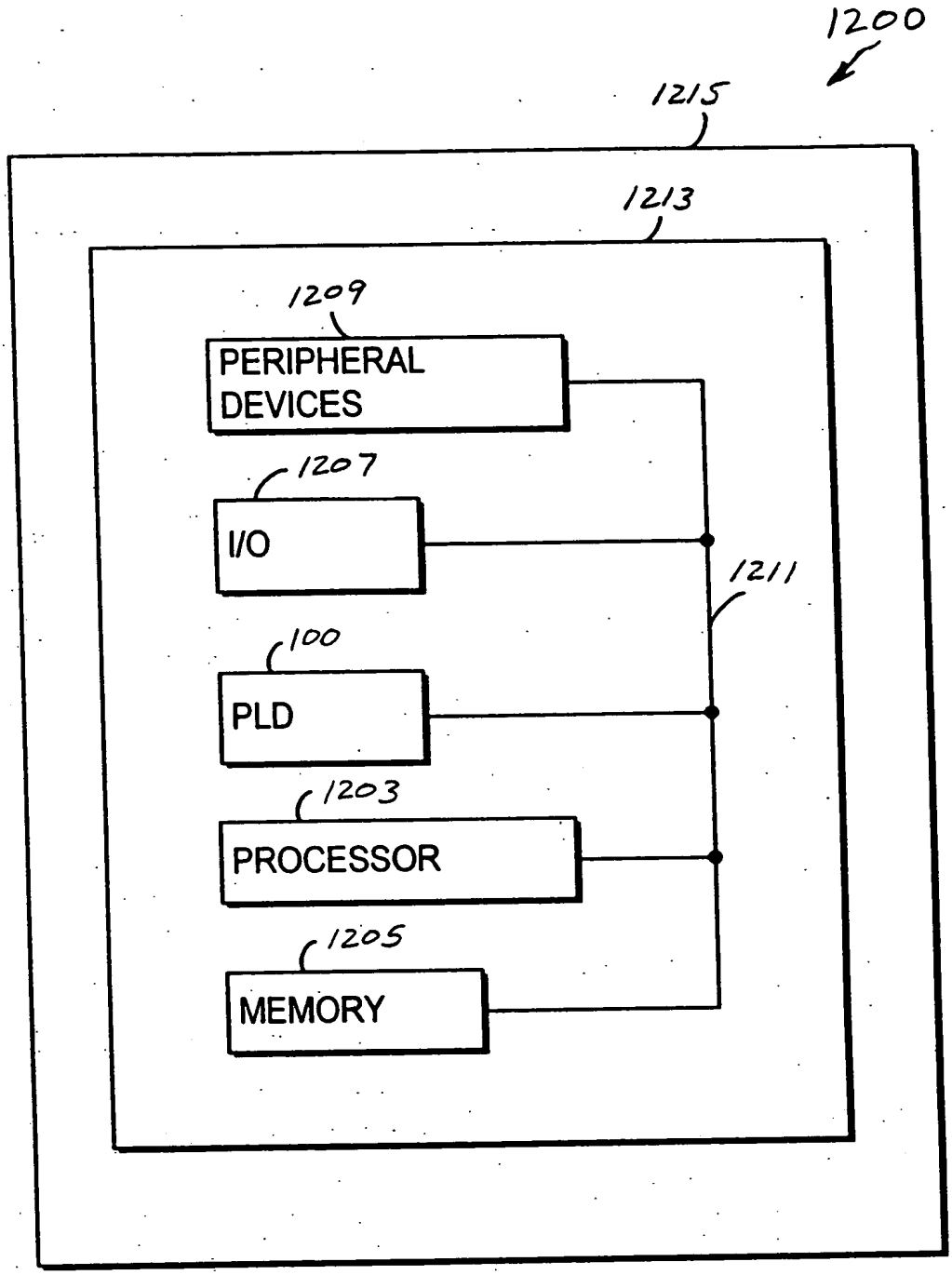
1200
1215
1213
1209
PERIPHERAL DEVICES
1207
I/O
1211
100
PLD
1203
PROCESSOR
1205
MEMORY

FIG. 12